IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) An apparatus ~~being connected~~for connection between a display device and a processor controlling the display device, comprising:

a memory bus ~~connected~~for connection to the processor, and

an adaptor circuit ~~connected~~for connection between the memory bus and a display device connection interface, said display device connection interface being integrated in the display device,

~~wherein the apparatus is configured to realize signaling between the processor and the display device connection interface, and~~

~~wherein the adapter circuit is configured to match signals between the memory bus and the display device connection interface by synchronizing the signals of the memory bus in an order required by the display device~~wherein the memory bus provides the adaptor circuit a plurality of control signal lines for writing or reading data to or from the display device, and a plurality of data signal lines carrying the data,

wherein the adaptor circuit provides the display device connection interface a read signal line, a write signal line, an address signal line indicating where on the display device the data should be read or written, and a plurality of data signal lines carrying the data,

and wherein the adaptor circuit is configured to convert an update instruction from the processor into an instruction to the display device in a timing order required by the display device for updating only a required part of the display device.

2. (Previously presented) The apparatus according to claim 1, wherein the display device connection interface is a medium speed screen interface.

3. (Previously presented) The apparatus according to claim 1, wherein the memory bus connected to the processor is a non-synchronized memory bus.

4. (Previously presented) The apparatus according to claim 1, wherein the memory bus is configured to realize signaling between the processor and a memory unit, as well as between the processor and the display device connection interface.

5. (Canceled)

6. (Previously presented) The apparatus according to claim 1, wherein the adapter circuit comprises one or more gates, said gates are configured to match respective signals between the memory bus and the display device connection interface.

7. (Previously presented) The apparatus according to claim 1, further comprising an interference protection block connected between the adapter circuit and the display device connection interface, said interference protection block being configured to prevent electric interferences among signals.

8. (Currently amended) A method, comprising:

establishing a connection between a memory bus and a display device connection interface, wherein said display device connection interface is integrated in a display device; and

converting an update instruction from a processor controlling the display device into an instruction to the display device in a timing order required by the display device for updating only a required part of the display device,

~~matching signals between the memory bus and the display device,~~

wherein the memory bus is connected between ~~a~~ the processor controlling the display device and an adapter circuit, said adapter circuit is connected between the memory bus and the display device connection interface,

wherein the memory bus provides the adaptor circuit a plurality of control signal lines for writing or reading data to or from the display device, and a plurality of data signal lines carrying the data, and

wherein the adaptor circuit provides the display device connection interface a read signal line, a write signal line, an address signal line indicating where on the display device the data should be read or written, and a plurality of data signal lines carrying the data ~~and~~

~~wherein matching the signals between the memory bus and the display device comprises synchronizing the signals of the memory bus in an order required by the display device by said adapter circuit~~.

9. (Previously presented) The method according to claim 8, wherein the memory bus connected to the processor is configured to function both as a bus between the processor and a memory unit, and a bus between the processor and the display device.

10. (Canceled)

11. (Previously presented) The method according to claim 8, wherein the memory bus and the display device connection interface are connected by glue logics together in order to achieve communication therebetween.

12. (Currently amended) An adapter circuit, ~~connected~~for connection between a memory bus and a display device connection interface integrated in a display device,

wherein said memory bus is for connection to a processor controlling the display device and it provides the adaptor circuit a plurality of control signal lines for writing or reading data to or from the display device, and a plurality of data signal lines carrying the data, ~~having one or more control signal lines and one or more data signal lines for realizing signaling between a processor and the display device,~~

wherein the adaptor circuit provides the display device connection interface a read signal line, a write signal line, an address signal line indicating where on the display device the data should be read or written, and a plurality of data signal lines carrying the data, and

wherein said adapter circuit is configured to convert an update instruction from the processor controlling the display device into an instruction to the display device in a timing order required by the display device for updating only a required part of the display device. ~~match signals between the memory bus and the display device by synchronizing the signals of the memory bus in an order required by the display device~~.

13. (Previously presented) The adapter circuit according to claim 12, wherein the adapter circuit is provided with gates for synchronizing the timing of the signals between the display device connection interface and the memory bus, and for combining the display device connection interface and the memory bus as a physical, uniform bus.

14. (Previously presented) The method of claim 8, wherein the adapter circuit is provided with gates in order to match the signals between the memory bus and the connection interface.